



IBM, CHARTERED EXTEND 90-NANOMETER COMMON PLATFORM WITH LOW-POWER DESIGN SOLUTIONS, HIGH-SPEED CONNECTIVITY CORES

Addition of low-power library, reference flows, and critical cores enhances sourcing flexibility for leading-edge 90nm designs

EAST FISHKILL, N.Y. and SINGAPORE – May 25, 2005 – IBM and Chartered Semiconductor Manufacturing today announced a further expansion of their jointly developed 90-nanometer (nm) process platform with the addition of common design enablement support. The additional support includes power-optimized, manufacturing-aware libraries; low-power electronic design automation (EDA) reference flows; and design kits for critical high-speed connectivity interface standards, including USB 2.0 and PCI Express.

Expanded support – provided by ARM®, Cadence Design Systems, Inc., Magma Design Automation Inc. and Synopsys, Inc – augments the existing ecosystem of support for the IBM-Chartered 90nm base process platform and underscores the companies' expanding efforts to help early adopters reduce design risks and achieve fast volume ramp for their leading-edge system-on-chip (SoC) products.

Extending ARM's current library support for the 90nm base process at IBM and Chartered, ARM's Artisan® Metro™ low-power libraries – a suite of standard cells, memory generators, and general purpose and specialty I/O cells developed and optimized for low-power design – are immediately available as the initial foundation library offering to support low-power processes and third-party low-power reference flows.

Cadence, Magma and Synopsys are collaborating with Chartered and IBM to provide low-power reference flows for the 90nm common platform. The validation process involves running both a high-level block-based design and more complex SoC design through the reference flows to demonstrate important low-power design techniques while achieving electromigration, signal integrity and timing closure requirements.

Upon availability, the reference flows, coupled with the libraries will support a variety of power reduction methodologies – multi-voltage threshold design, voltage scaling and voltage islands – and therefore help enable a more efficient and effective way to design to the 90nm low-power process platform. (See separate releases from Cadence, Magma and Synopsys.)

To provide design enablement for high-speed interface standards, IBM and Chartered intend to offer design kits for their jointly developed 90nm process that support Synopsys' USB 2.0 Physical Layer core (PHY IP) and ARM's Velocity™ Serial Link PHY IP for supporting specifications such as PCI Express, Serial ATA, SAS, and XAUI. The design kits will include a comprehensive set of views and models required by EDA tools to support designers with their early design exploration. (See separate releases from ARM and Synopsys.)

"IBM and Chartered's jointly developed process continues to gain acceptance with both customers and other companies in the value-chain. Broadening the commonality of the platform is helping it emerge as the standard that partners and design solutions companies are targeting with new capabilities," said Steve Longoria, vice president, Semiconductor Technology Platform for IBM. "The addition of these critical elements for leading-edge design addresses pressing issues for early adopters of 90nm process technology, namely low power and high-speed connectivity applications."

Both the low-power design and high-performance cores benefit from a comprehensive validation approach. A team comprised of IBM and Chartered technical experts worked closely with design enablement companies to accelerate the development of technology files and scripts as well as provide access to critical manufacturing data for more accurate design kits and reference flows. The collaboration also extended to comprehensive design rule checking (DRC); layout versus schematic (LVS) matching; and design for manufacturability (DFM) and design for yield (DFY) analysis and review.

"We now have the advantage of a well-defined and thorough approach, which is enabling us to offer new and validated 90nm EDA and IP support faster," said Kevin Meyer, vice president of worldwide marketing at Chartered. "We continue to enhance

the design enablement support for 90nm even as we move to 65nm and beyond, which should result in earlier availability for leading-edge adopters of new technology."

About IBM

IBM is the world's largest information technology company, with 80 years of leadership in helping businesses innovate. Drawing on resources from across IBM and key IBM Business Partners, IBM offers a wide range of services, solutions and technologies that help enable customers, large and small, to take full advantage of the new era of e-business on demand. For more information about IBM, visit http://www.ibm.com. For more information on IBM's on demand strategy, visit http://www.ibm.com/ondemand.

About Chartered

Chartered Semiconductor Manufacturing (Nasdaq: CHRT, SGX-ST: CHARTERED), one of the world's top dedicated semiconductor foundries, offers leading-edge technologies down to 90 nanometer (nm), enabling today's system-on-chip designs. The company further serves its customers' needs through a collaborative, joint development approach on a technology roadmap that extends to 45nm. Chartered's strategy is based on open and comprehensive design enablement solutions, manufacturing enhancement strategies, and a commitment to flexible sourcing. In Singapore, the company operates a 300mm fabrication facility and four 200mm facilities. Information about Chartered can be found at www.charteredsemi.com.

Chartered is a founding member of Power.org, an open standards community formed in December 2004 around chips and systems, which use Power Architecture technology.

Chartered Safe Harbor Statement under the provisions of the United States Private Securities Litigation Reform Act of 1995

This news release contains forward-looking statements, as defined in the safe harbor provisions of the U.S. Private Securities Litigation Reform Act of 1995. These forward-looking statements, including without limitation, the statements relating to the expected availability of the low-power reference flows; customers and partners' acceptance of the IBM-Chartered common process platform in the value-chain; and the expected results of our continued enhancement of design enablement support for 65-nm and beyond reflect our current views with respect to future events and are subject to certain risks and uncertainties, which could cause actual results to differ materially from historical results or those anticipated. Among the factors that could cause actual results to differ materially are: changes in market outlook and trends; demands from our major customers, excess inventory and life cycles of specific products; competition from other foundries; unforeseen delays or interruptions in our plans for our fabrication facilities; the performance level of and technology mix in our fabrication facilities; our progress on leading edge products; the successful implementation of our joint development agreement with IBM; the successful implementation of our collaborative efforts with our design enablement partners; the timing and rate of the semiconductor market recovery; economic conditions in the United States as well as globally and the growth of fables companies and the outsourcing strategy of integrated device manufacturers. Although we believe the expectations reflected in such forward-looking statements are based upon reasonable assumptions, we can give no assurance that our expectations will be attained. In addition to the foregoing factors, a description of certain other risks and uncertainties which could cause actual results to differ materially can be found in the section captioned "Risk Factors" in our Annual Report on Form 20-F filed with the U.S. Securities and Exchange Commission. You are cautioned not to place undue reliance on these forward-looking statements, which are based on the current view of management on future events. We undertake no obligation to publicly update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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